**Sirius DVP clock delay chain design**

1. Function:

Delay the clock input for parallel video data input.

1. Cell use:

SVP\_DEL\_L4\_1

SVP\_DEL\_L4V1\_1

SVP\_DEL\_L6\_1

SVP\_BUF\_S\_1

1. Total phases

32 phases, the max input clock frequency is 150MHz

1. Block diagram
   1. For each phase unit, it contains 2\*SVP\_DEL\_L6\_1, 1\*SVP\_DEL\_L4V1\_1, 3\*SVP\_BUF\_S\_1, 1\*SVP\_BUF\_S\_2, 2\*SVP\_BUF\_S\_4



Delay\_unit



Delay chain



Mux\_16



Mux\_2 for clk out

All mux is SVP\_MUX2\_1, and the last output used SVP\_BUF\_S\_4.

1. PHASE select

For DVP0 , mux\_sel[4:0] is 0x645b258 [5:0]

For DVP1 , mux\_sel[4:0] is 0x645b258 [11:6]

1. Delay analyze

|  |
| --- |
| For corner ff -40, 32 phase takes 1.2 of tt delay time |
| For corner ss -40, 32 phase takes 4.6 of tt delay time |
| For corner tt, 32 phase takes about 2.0 cycle. (150M) |